

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.

PATENT DATE

SCANNED

Q.A.

APPLICATION NO. 09/939636	CONT/PRIOR	CLASS 257	SUBCLASS 25	ART UNIT 2815	EXAMINER
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Kevin Devereaux

APPLICANTS

III

Method and apparatus for wafer level testing of semiconductor using sacrificial on die power and ground metalization

PTO-2040
12/99

ISSUING CLASSIFICATION										
ORIGINAL				CROSS REFERENCE(S)						
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
INTERNATIONAL CLASSIFICATION										

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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner)		NOTICE OF ALLOWANCE MAILED _____	
<input checked="" type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	_____ (Primary Examiner)		ISSUE FEE Amount Due: _____ Date Paid: _____	
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<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)		_____ (Date)	

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